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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	PERVEZ H. SAGARWALA ET AL
Serial No.	:	09/800,039
Filed	:	March 6, 2001
For	:	CMOS INTEGRATED CIRCUIT DEVICE WITH LDD N-CHANNEL TRANSISTOR AND NON-LDD P-CHANNEL TRANSISTOR
Group No.	:	2822
Examiner	:	M.V. Prenty

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6/4/03

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Commissioner for Patents
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Sir:

APPELLANTS' BRIEF ON APPEAL

This Brief is submitted in triplicate on behalf of Appellants for the application identified above.

A Petition for Extension of Time (1 mo.) and a Supplemental Amendment and Response to Final Office action are concurrently submitted herewith.

A check in the amount of $320.00 is enclosed for the Appeal Brief filing fee. A check in the amount of $110.00 is enclosed for the Extension of Time filing fee. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

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REAL PARTY IN INTEREST

The real party in interest for this appeal is the assignee of the application, STMICRO-ELECTRONICS, INC. (f/k/a SGS-THOMSON MICROELECTRONICS, INC.).

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present application which are currently pending.

STATUS OF CLAIMS

Claims 1–7 and 27–39 are pending in the present application. Claim 27 was rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Claims 1–7 and 28–39 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claims 33–34 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,273,914 to *Miyajima et al.* Claims 27–30 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,766,991 to *Chen*. The rejection of pending claims 1–7 and 27–39 is appealed.

STATUS OF AMENDMENTS

An amendment is being submitted herewith to overcome a pending rejection. No other amendments to the claims were submitted following the final Office Action mailed November 8, 2002.

SUMMARY OF THE INVENTION

The present invention relates to formation of complementary metal-oxide-semiconductor (CMOS) circuits within a substrate. At the time the invention was conceived, conventional CMOS processing techniques included use of removable sidewall spacers to form lightly doped drain (LDD) extensions to transistor source and drain regions near the gate of both p-channel and n-channel transistors to improve performance. Specification, page 2, lines 11–15. However, use of removable sidewall spacers requires extra masking and etch steps during processing. Specification, page 3, line 15 through page 6, line 6.

In the present invention, processing steps are saved by forming LDD regions only for n-channel transistors, since p-channel transistors remain reliable at shorter channel lengths without LDD regions than n-channel transistors:

> LDD regions are used in the manufacture of MOS devices because as device size, and particularly channel length, is reduced, conventional drain structure MOS devices can become unreliable due to short channel effect, such as hot carrier effects. Conventional drain structure p-channel MOS devices remain reliable at shorter channel lengths than conventional drain structure n-channel MOS devices.

Specification, page 10, lines 3–8. However, consideration must also be given to the channel length (the distance between the source and drain) since the transistor will not operate reliably due to short channel effects when the channel length is below a minimum and will not turn on efficiently when the channel length is above a maximum:

> Referring to FIG. 11, a MOS device, manufactured using CMOS technology, is reliable when the distance 70 between its source and drain 44', i.e. its channel length, is between a minimum length and a maximum length. The minimum length is a distance between the source and drain of the transistor below which the transistor will not operate reliably due to short channel effects when a conventional voltage is applied to the gate electrode. The maximum length is the distance between the source and drain of the transistor above which the transistor will not turn on efficiently. The transistor will not turn on efficiently when current does not flow between the source and drain of the transistor when a conventional voltage is applied to the gate electrode of the transistor. The minimum and maximum lengths are dependent on the gate length, spacer length, diffusion cycles, and junction depth of the implant. Conventional voltage is typically 5, 3.3, or 2.7 volts in current technology.

Specification, page 10, lines 8–20. Of course, using LDD regions alters the minimum and maximum channel lengths for a transistor (as opposed to not forming such regions as part of the transistor structure):

> When an LDD region is used, the length 72 between low resistivity regions of the source and drain regions 54 has to be between a minimum LDD length and a maximum LDD length. The minimum LDD length is a distance between the low resistivity regions 56 of the source and drain regions 54 of the transistor below which the transistor will not operate reliably due to short channel effects. The maximum LDD length is the distance between the low resistivity regions of the source and drain regions 54 of the transistor above which transistor will not turn on efficiently. The transistor will not turn on efficiently when current does not flow between the source and drain of the transistor when a conventional voltage is applied to the gate electrode 22 of the transistor. In current technology, for an n-channel device

> manufactured using CMOS technology, the n-channel minimum LDD length and the n-channel maximum LDD length is typically primarily based on the doping concentration of the impurity forming the LDD and the LDD length.

Specification, page 10, lines 23–25. The challenge, therefore, is to form a transistor structure having one channel length 70 for p-channel transistors without LDD regions and a second, different channel length 72 for n-channel transistors having LDD regions, but without requiring an excessive number of processing steps:

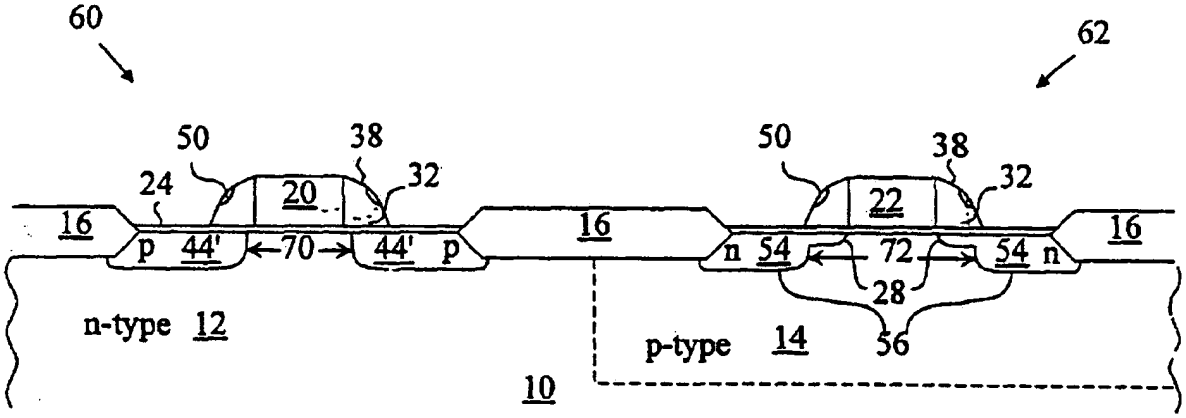


Figure 11

Specification, Figure 11.

In the present invention, such differing channel lengths for p-channel and n-channel transistors are achieved without excessively complicated processing by using two insulating layers to tailor the lengths of the channel lengths. Specification, page 11, lines 12–16. A structure is

formed having LDD regions 28 implanted adjacent a gate electrode 22 for the n-channel transistor and a gate 20 (without adjacent LDD regions) for the p-channel transistor:

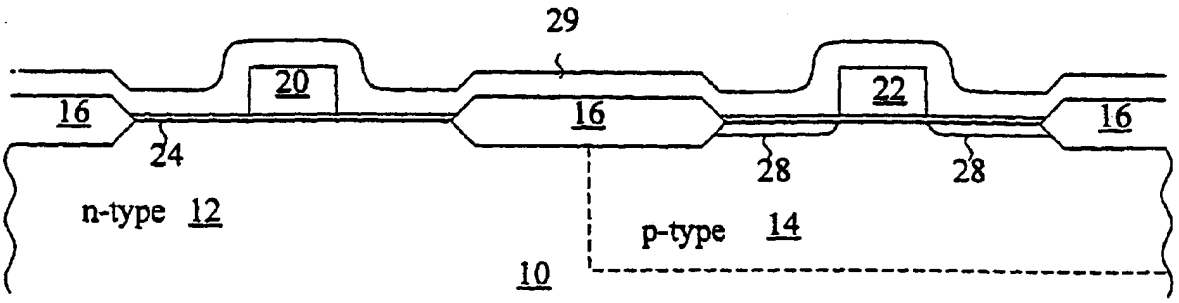


Figure 6

Specification, Figure 6, page 12, line 3 through page 13, line 3. The width of gate electrode 20 for the p-channel transistor is less than the minimum channel length of the p-channel transistor. Specification, page 17, lines 5–10. To space the source and drain regions for the p-channel transistor a proper distance apart, a first conformal insulating layer 29 is formed over the entire structure. Specification. Page 13, lines 5–8. The thickness of insulating layer 29 is sufficient that the portions on sidewalls of the gate electrode 20, combined with the width of the gate electrode 20, equal or exceed the minimum channel length required for the p-channel transistor. Specification, page 13, lines 8–13. The thickness of insulating layer 29 should also take into account diffusion of the implanted source and drain regions for the p-channel transistor during later processing steps. Specification, page 15, lines 11–15.

Source drain regions 44 are then implanted through the insulating layer 29 into the area 12 of the p-channel transistor (but not into the area 14 of the n-channel transistor due to mask 42), masked by the gate electrode 20 and the portions of insulating layer 29 on sidewalls of gate electrode:

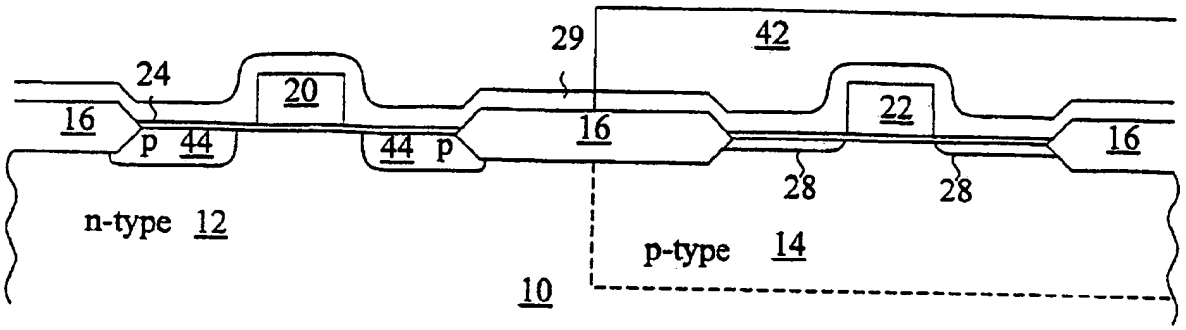


Figure 7

Specification, Figure 7, page 13, lines 15–21. Due to the portions of insulating layer 29 on sidewalls of the gate electrode 20, source and drain regions 44 for the p-channel transistor are spaced apart by at least the minimum required channel length for the p-channel transistor.

A second conformal insulating layer 48 is then deposited over the entire structure:

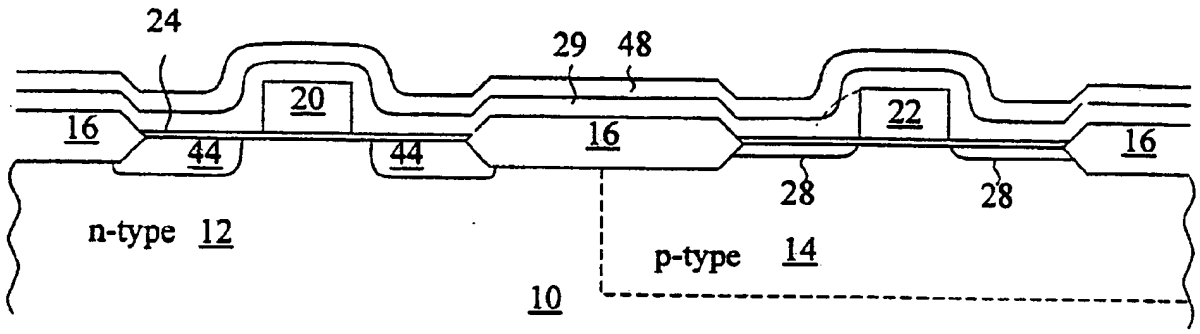


Figure 8

Specification, Figure 8, page 13, lines 23–26. The second insulating layer 48 is formed to a thickness sufficient, with the thickness of insulating layer 29, to form sidewall spacers of a desired width, such that the combined width of the sidewall spacers and the gate electrode 22 exceeds the minimum required channel length for the n-channel transistor (with LDD regions). Specification, page 13, line 26 through page 14, line 4. The insulating layers 29 and 38 are anisotropically etched to form sidewall spacers 32 beside both electrodes 20 and 22, each sidewall spacer including a first region or portion 32 from the first insulating layer 29 and a second region or portion 50 from the second insulating layer 48:

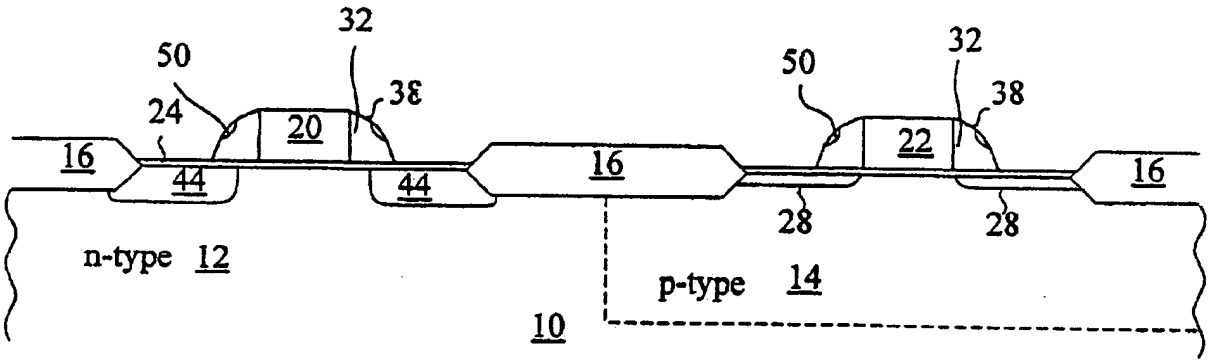


Figure 9

Specification, Figure 9, page 14, lines 6–9. The width of sidewall spacers 32, combined with the width of gate electrode 22 for the n-channel transistor, exceeds minimum channel length required for the n-channel transistor. Specification page 14, lines 9–14.

Source and drain regions 54 are then implanted through the LDD regions 28 within the area 14 of the n-channel transistor (with mask 68 protecting the area 12 of the p-channel transistor), masked by sidewalls 32:

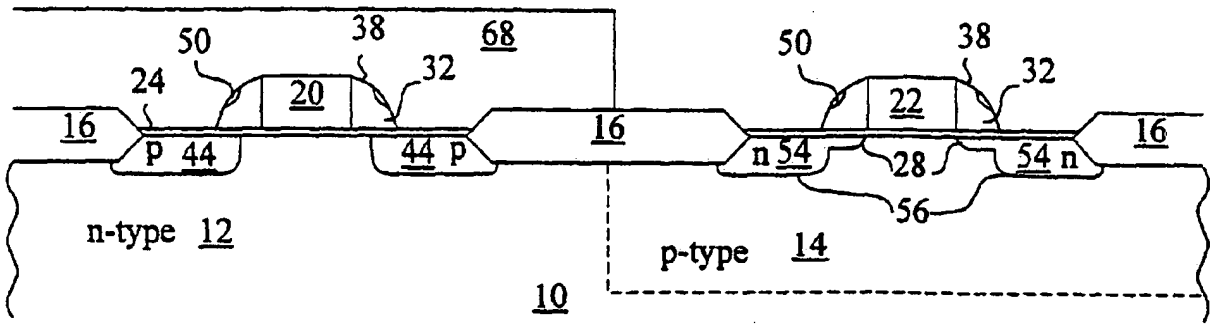


Figure 10

Specification, Figure 10, page 14, lines 16–20. The resulting structure, shown in Figure 11 above, includes a p-channel transistor with a gate electrode less than a minimum channel length for the p-channel transistor and sidewall spacers each formed with two portions, from the two insulating layers 29 and 48.

ISSUES ON APPEAL

Claims 1–7 and 27–39 are pending in the present application. Claim 27 was rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Claims 1–7 and 28–39 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claims 33–34 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Miyajima et al.*

Claims 27–30 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen*. The issues on appeal are:

1. Whether claim 27 was properly rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention;

2. Whether claims 1–7 and 28–39 were properly rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention;

3. Whether claims 33–34 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,273,914 to *Miyajima et al*; and

4. Whether claims 27–30 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,766,991 to *Chen*.

GROUPING OF CLAIMS

Claims 1–7 and 27–39 are pending in the present application. Claim 27 was rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Claims 1–7 and 28–39 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to

particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claims 33–34 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Miyajima et al.* Claims 27–30 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen*. For purposes of this appeal, the pending claims will be grouped together as follows:

Group A – claims 1, 28–30, 32–33 and 35;

Group B – claims 5–6;

Group C – claims 30 and 35;

Group D – claim 27;

Group E – claims 33–34;

Group F – claims 27–32;

Group G – claims 28–32;

Group H – claim 29;

Group I – claim 30; and

Group J – claim 31.

Groups A–J stand or fall independently. Patentability of the claims within each group is argued separately below.

ARGUMENT

Group A (Claims 1, 28–30, 32–33 and 35)

Claims 1, 28–30, 32–33 and 35 of Group A were rejected under 35 U.S.C. § 112, second paragraph, were rejected as being indefinite. These claims are properly grouped together and considered separately from the claims of Groups B–J because the claims are subject to a different grounds of rejection than the claims of Groups B–J.

Claims 1, 28–30, 32–33 and 35 of Group A were rejected as indefinite for reciting "a minimum channel length required for the p-channel transistor." The standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope. MPEP § 2173.02. If the scope of the subject matter embraced by the claims is clear, then the claims comply with 35 U.S.C. § 112, second paragraph. MPEP § 2173.04.

As taught in the specification and well known in the relevant art, the minimum length for a transistor is a distance between the (low resistivity) source and drain below which the transistor will not operate reliably due to short channel effects when a conventional voltage (typically 5, 3.3 or 2.7 volts) is applied to the gate electrode, and depends on gate and spacer length, diffusion cycles and implant junction depth. Specification, page 10, lines 10–20. There is no indication in the record--nor does the Office Action identify any reason--that those skilled in the relevant art are incapable of determining a channel length and/or whether a particular channel length is above a minimum channel length for a particular fabrication process (implant energy, drive time, etc.).

Group B (Claims 5–6)

Claims 5–6 of Group B were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. These claims are properly grouped together and considered separately from the claims of Groups A and C–J because the claims are subject to a different grounds of rejection than the claims of Groups A and C–J.

Claims 5–6 of Group B were rejected as indefinite for reciting that the transistor channel length is greater than "a distance below which the transistor will not operate reliably due to short channel effects" (i.e., the minimum channel length) and less than "a distance above which the transistor will not turn on efficiently" (i.e., the maximum channel length). As taught in the specification and well known in the relevant art, the minimum and maximum channel lengths are dependent on gate and spacer length, diffusion cycles, and implant junction depth. Specification, page 10, lines 17–19. There is no indication in the record--nor does the Office Action identify any reason--that those skilled in the relevant art are incapable of determining a channel length and/or whether a particular channel length is above a minimum channel length and below a maximum channel length for a particular fabrication process.

Group C (Claims 30 and 35)

Claims 30 and 35 of Group B were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. These claims are properly grouped together and considered separately from the

claims of Groups A–B and D–J because the claims are subject to a different grounds of rejection than the claims of Groups A–B and D–J.

Claims 30 and 35 of Group C were rejected as indefinite for reciting that the channel length takes into account "a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor." As taught by the specification and well known in the relevant art, dopants implanted for the source and drain regions of the p-channel transistor may diffuse during subsequent high-temperature processing. Specification, page 13, lines 7–11. There is no indication in the record--nor does the Office Action identify any reason--that those skilled in the relevant art are incapable of determining a distance that implanted dopants will diffuse during particular processing steps (based on temperature, duration, existing doping profile, etc.).

Group D (Claim 27)

Claim 27 of Group D was rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not disclosed in the specification in such a way as to reasonably convey to those skilled in the relevant art that the inventor(s) had possession of the claimed invention at the time the application was filed. This claim is properly considered separately from the claims of Groups A–C and E–J because the claim is subject to a different grounds of rejection than the claims of Groups A–C and E–J.

Claim 27 is being amended herewith to obviate the written description rejection.

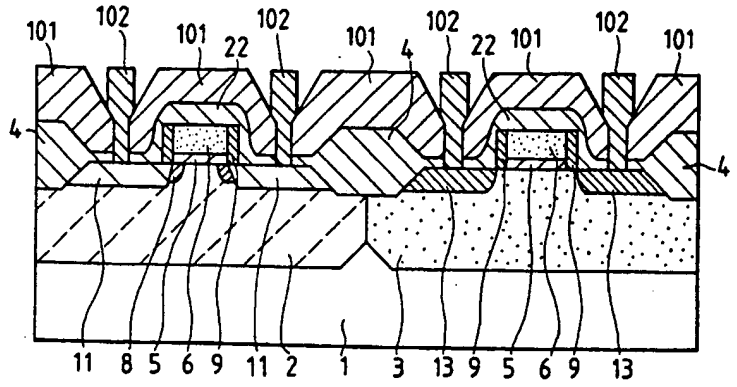
Group E (Claims 33–34)

Claims 33–34 of Group E were rejected under 35 U.S.C. § 102(b) as being anticipated by *Miyajima et al.* These claims are properly grouped together and considered separately from the claims of Groups A–D and F–J because the claims are subject to a different grounds of rejection than the claims of Groups A–D and F–J.

Claims 33–34 of Group E were rejected under 35 U.S.C. § 102(b) as being anticipated by *Miyajima et al.* A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-69 (8th ed. August 2001).

Independent claim 33 of Group E recites "a gate electrode overlying a portion of the n-type region, the gate electrode having a width less than a minimum channel length required for the p-channel transistor" and "at least one conformal insulating layer over a top and sides of the gate electrode, the insulating layer having a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds a minimum channel length required for the p-channel transistor." Such a feature is not found in the cited reference. The embodiments of Figures 13(g) and 13(h) in *Miyajima et al* depict a gate electrode 6 having a width less than a channel length of a p-channel transistor, and an oxide 22 over the gate electrode 6:

FIG. 13(h)



Miyajima et al, Figure 13(h), column 9, line 47 through column 10, line 27. However, *Miyajima et al* is silent as to whether the thickness of oxide 22, combined with the width of gate electrode 6, exceeds a minimum channel length required for the transistor. Nor can such a feature be inferred from the disclosure since *Miyajima et al* discloses sidewalls 9 between gate electrode 6 and oxide layer 22.

Group F (Claims 27–32)

Claims 27–32 of Group F were rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen et al.* These claims are properly grouped together and considered separately from the claims of Groups A–E and G–J because the claims are subject to a different grounds of rejection than the claims of Groups A–E and G–J, and since a favorable decision with respect to the claims of Group F may obviate the need for consideration of the claims of Groups G–J.

Independent claims 27–28 of Group F each recite forming a p-channel transistor without lightly doped source and drain regions. Such a feature is not found in the cited reference. *Chen et al* describes a process for forming a CMOS transistor structure, and depicts the structure at various points during processing in Figures 2–10, which include lightly doped source and drain regions. *Chen et al* also discloses two "variants" of the process, described in connection with Figures 11–12 and Figure 13, respectively. In these variants, alternative processes to the steps within the "main" process that form the p+ (heavily doped) regions of the p-channel transistor are described. However, *Chen et al* is silent as to terminating the variants after the steps depicted in Figures 12 or 13--that is, NOT subsequently forming the lightly doped source and drain regions. Instead, *Chen et al* merely describes the differences in the variants from the "main" process, rather than set forth the entire process three times. The self-aligned lightly doped source and drain regions depicted in Figure 9 and described at column 5, lines 46–49 are presumably formed after the processing steps described in connection with Figures 12 and 13.

In addition, independent claim 27 of Group F each recite that the gate electrode for the p-channel transistor has a width less than a channel length of the p-channel transistor. Similarly, independent claim 28 recites that the gate electrode has a width less than a minimum channel length for the p-channel transistor. Such a feature is not found in the cited reference. *Chen et al* teaches self-aligned lightly doped source and drain regions that, as described above, are presumably formed

for all three variants, forming a channel having a length at least equal to if not less than the gate width (i.e., the gate width is equal to or greater than the channel length).

Finally, independent claim 27 of Group F recites sidewall spacers including first and second regions and overlying a portion of the channel. Similarly, independent claim 28 of Group F recites first sidewall spacers (or sidewall spacer regions) overlying at least a portion of the channel for the p-channel transistor. Such a feature is not found in the cited reference. *Chen et al* teaches, for all three variants, channel regions self-aligned to the gate electrode, which precludes sidewalls from overlying the channel.

Group G (Claims 28–32)

Claims 28–32 of Group G were rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen et al*. These claims are properly grouped together and considered separately from the claims of Groups A–F and H–J because the claims are subject to a different grounds of rejection than the claims of Groups A–E and G–J and since the claims contains a common limitation distinguishing the claimed invention over the cited reference that is not found in the remaining claim of Group F.

Independent claim 28 of Group G recites a p-channel transistor gate electrode having a width less than a minimum channel length (i.e., not just less than the actual channel length) for the p-channel transistor. Such a feature is not found in the cited references. As noted above, *Chen et al* disclose self-aligned source and drain regions for the p-channel transistor. *Chen et al* is silent as to

whether the gate electrode width is less than a minimum channel length for the p-channel transistor. Nor can such a limitation be inferred from the structure depicted and described by *Chen et al.*

Group H (Claim 29)

Claim 29 of Group H was rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen et al.* This claim is properly considered separately from the claims of Groups A–G and I–J because the claim is subject to a different grounds of rejection than the claims of Groups A–E and since the claim contains a limitation distinguishing the claimed invention over the cited reference that is not found in the remaining claims of Groups F–G.

Claim 29 of Group H recites that the first sidewall spacer regions have a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode (which is less than a minimum channel length for the p-channel transistor), exceeds a minimum channel length for the p-channel transistor. Such a feature is not found in the cited reference. *Chen et al* is silent as to such a feature and, since only self-aligned source and drain regions are disclosed, such a limitation cannot be inferred from the disclosed structure.

Group I (Claim 30)

Claim 30 of Group I was rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen et al.* This claim is properly considered separately from the claims of Groups A–H and J because the claim is subject to a different grounds of rejection than the claims of Groups A–E and since the claim

contains a limitation distinguishing the claimed invention over the cited reference that is not found in the remaining claims of Groups F–H.

Claim 30 of Group G recites that the thickness of the first sidewall spacers (or spacer regions), taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor plus a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor. Such a feature is not found in the cited reference.

Group J (Claim 31)

Claim 31 of Group J was rejected under 35 U.S.C. § 102(e) as being anticipated by *Chen et al.* This claim is properly considered separately from the claims of Groups A–I because the claim is subject to a different grounds of rejection than the claims of Groups A–E and since the claim contains a limitation distinguishing the claimed invention over the cited reference that is not found in the remaining claims of Groups F–I.

Claim 31 of Group J recites second sidewall spacers (or spacer regions) adjacent the first sidewall spacers (spacer regions) and overlying the source and drain regions for the p-channel transistor. Such a feature is not found in the cited reference. *Chen et al* explicitly teaches removal of the silicon nitride regions 78 and 79, in preparation of forming the lightly doped source and drain regions.

CONCLUSION

The claims of Groups A–C are not indefinite. Therefore, the rejection under 35 U.S.C. § 112, second paragraph is improper. The claim of Group D was amended to overcome the rejection under 35 U.S.C. § 112, first paragraph. None of the cited references, taken alone or in combination, depict or describe all features of the invention claimed in Groups E–J. Therefore, the rejections under 35 U.S.C. § 102 is improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting all pending claims in the application.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 5-27-03

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APPENDIX TO APPELLANT'S BRIEF ON APPEAL
PENDING CLAIMS ON APPEAL

1. A CMOS integrated circuit device comprising:

a plurality of p-channel transistors formed in active surface areas of n-type regions, wherein the p-channel transistors do not have LDD source/drain regions;

a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;

gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and being insulated from the respective active surface areas, wherein the gate electrodes for the p-channel transistors have a width less than a minimum channel length required for the p-channel transistors;

p-type source and drain regions for the p-channel transistors, each p-type source and drain region consisting of a low resistivity region;

n-type source and drain regions for the n-channel transistors, each n-type source and drain region having a low resistivity region and an LDD region;

each gate electrode having a pair of sidewall spacers each having an inner and an outer portion, wherein the inner portions of the sidewall spacers for each p-channel transistor gate electrode has a width which, taken on each side of the respective gate electrode for the respective p-channel transistor and combined with the width of the respective gate electrode for the respective p-channel transistor, exceeds a minimum channel length for the respective p-channel transistor;

each p-channel low resistivity region located under the outer portion and at least a part of the

inner portion of its respective sidewall spacer;

each n-channel low resistivity region located under at least a part of the outer portion and a part of the inner portion of its respective sidewall spacer; and

each n-channel LDD region extending from its respective low resistivity region to underlie the inner portion of its respective sidewall spacer.

2. The integrated circuit of claim 1, wherein the inner portion of the sidewall spacer comprises an oxide.

3. The integrated circuit of claim 1, wherein the inner portion of the sidewall spacer comprises an oxide.

4. The integrated circuit of claim 1, wherein the p-channel source and drain comprise silicon implanted wtih BF_2.

5. The integrated circuit of claim 1, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the transistor will not operate reliably due to short channel effects; and

the p-channel maximum length is a distance above which the transistor will not turn on efficiently.

6. The integrated circuit of claim 1, wherein:

the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length, wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor will not turn on efficiently.

7. The integrated circuit of claim 1, wherein the sidewall spacers have a total width of approximately 500 to 2500 Å.

27. A CMOS integrated circuit structure, comprising:

an n-channel transistor including lightly doped source and drain regions within a p-type region of a substrate; and

a p-channel transistor without lightly doped source and drain regions within an n-type region of the substrate, the p-channel transistor including:

a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and

first and second sidewall spacers adjacent opposing sides of the gate electrode and overlying a portion of the channel for the p-channel transistor and portions of source and drain regions for the p-channel transistor.

28. A CMOS integrated circuit structure, comprising:

an n-channel transistor including lightly doped source and drain regions within a p-type region of a subdstrate; and

a p-channel transistor without lightly doped source and drain regions within an n-type region of the substrate, the p-channel transistor including:

a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and

first sidewall spacers adjacent opposing sides of the gate electrode and overlying at least a portion of the channel for the p-channel transistor and portions of source and drain regions for the p-channel transistor,

wherein the width of the gate electrode is less than a minimum channel length required for the p-channel transistor.

29. The CMOS integrated circuit structure of claim 28, wherein the first sidewall spacers have a width which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor.

30. The CMOS integrated circuit structure of claim 29, wherein the width of the first sidewall spacers, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor plus a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor.

31. The CMOS integrated circuit structure of claim 30, further comprising:

second sidewall spacers adjacent the first sidewall spacers and overlying source and drain regions for the p-channel transistor.

32. The CMOS integrated circuit structure of claim 30, wherein the n-channel transistor further comprises:

a gate electrode having a width approximately equal to a minimum channel length required for the n-channel transistor; and

sidewall spacers adjacent to opposing sides of the n-channel transistor gate electrode and overlying the lightly doped source and drain regions.

33. An intermediate structure for use in forming a CMOS integrated circuit, comprising:

a p-type region for an n-channel transistor including lightly doped source and drain regions;

an n-type region for a p-channel transistor without lightly doped source and drain regions;

a gate electrode overlying a portion of the n-type region, the gate electrode having a width less than a minimum channel length required for the p-channel transistor; and

at least one conformal insulating layer over a top and sides of the gate electrode, the insulating layer having a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds a minimum channel length required for the p-channel transistor.

34. The intermediate structure of claim 33, wherein the insulating layer forms a mask for implanting source and drain regions for the p-channel transistor.

35. The intermediate structure of claim 34, wherein the insulating layer has a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds the minimum channel length required for the p-channel transistor plus a diffusion distance for implanted dopants forming the source and drain regions for the p-channel transistor.

36. The intermediate structure of claim 35, further comprising:

source and drain regions for the p-channel transistor within the n-type region, wherein edges of the source and drain regions are spaced apart from the sides of the gate electrode.

37. The intermediate structure of claim 36, wherein the source and drain regions are low resistivity regions.

38. The intermediate structure of claim 33, further comprising:

second insulating layer overlying the first insulating layer to form sidewall spacers adjacent the gate electrode upon etching of the insulating layer and the second insulating layer.

39. The intermediate structure of claim 33, further comprising:

a n-channel transistor gate electrode overlying a portion of the p-type region;

lightly doped source and drain regions within the p-type region aligned with the n-channel transistor gate electrode.